เอกสารอ้างอิง

1. มนัส แซ่ด่าน. "การศึกษาปรากฏการณ์ฮอลล์ในสารกึ่งตัวนำโดยเทคนิคของแวน เดอร์พาว" วิทยานิพนธ์ปริญญามหาบัณฑิต ภาควิชาฟิสิกส์ บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย 2526

2. ยืน ภู่วรวรรณ และวัฒนา เชียงกูล. ไมโครโปรเซสเซอร์ ไมโครคอมพิวเตอร์ (Z-80 Microprocessor). พิมพ์ครั้งที่ 4, บริษัท ซีเอ็ดยูเคชัน จำกัด, กรุงเทพ, 2527.

3. Rodnay Zak, in Programming the Z-80. 3 th ed., pp 154-437, Sybex, Berkeley, 1983.

4. James W.Coffron. in Z-80 Applications. pp 163-187, Sybex, Berkeley, 1983.

5. National Semiconductor Corp., Data Conversion/Acquisition Databook, pp 5/14-5/43, National Semiconductor Corporation, Santa Clara, 1980.

6. Kittel, C. in Introduction to Solid State Physics, 5 th ed, pp 110-150, Wil ey & Sons, New York, 1956

ภาคผนวก ก. ข้อมูลจำเพาะของไดซีเบอร์ต่าง ๆ

SCL4081B, SCL4082B
SCL4073B

CMOS AND GATES

SCL4081B - Quad 2-Input AND
SCL4082B - Dual 4-Input AND
SCL4073B - Triple 3-Input AND

FEATURES

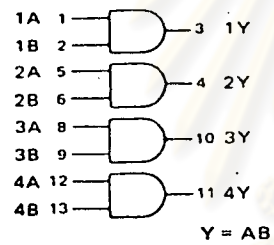
- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B" Series Compatible
- Balanced Output Drive Current Specifications

TRUTH TABLE

Inputs	Output
1 1 · · · 1	1
All other combinations	0

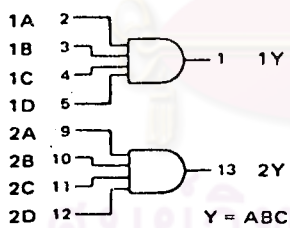
FUNCTION DIAGRAMS

SCL4081B



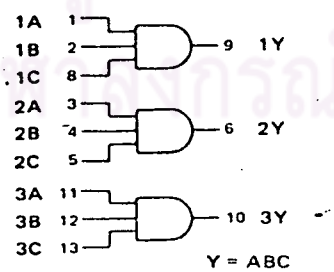
Y = AB

SCL4082B



Y = ABCD

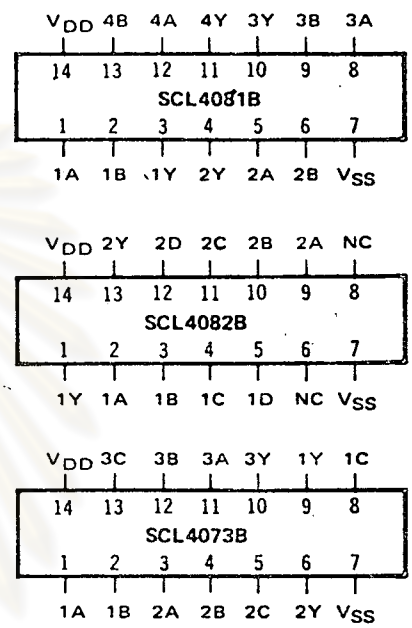
SCL4073B



Y = ABC

V_{DD} = Pin 14
V_{SS} = Pin 7
for all Devices

CONNECTION DIAGRAMS
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

ELECTRICAL CHARACTERISTICS

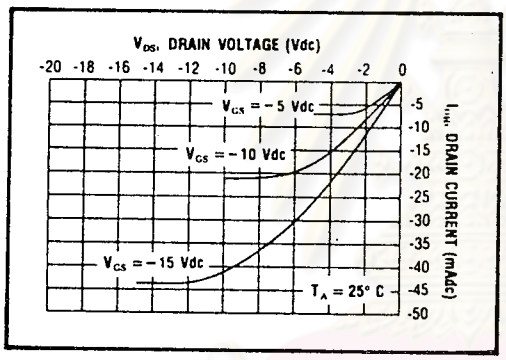
STATIC CHARACTERISTICS [1, 3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

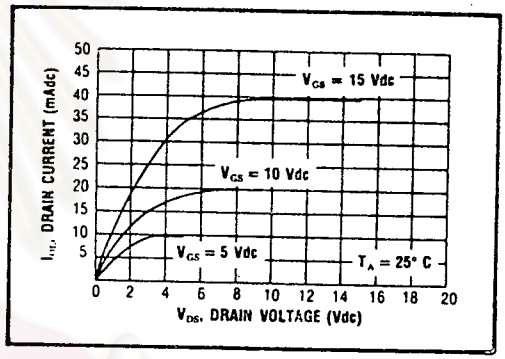
NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications"
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

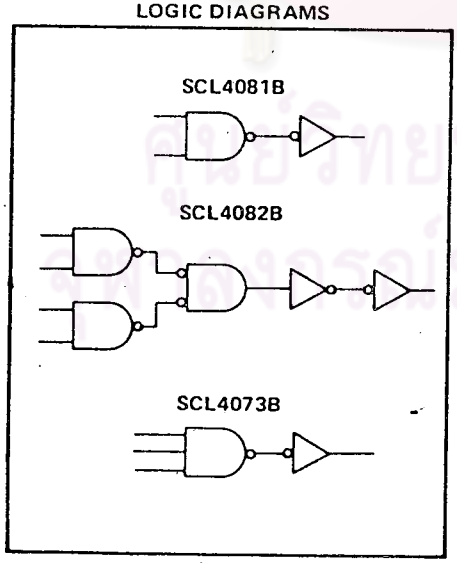


Typical P-Channel
Source Current Characteristics

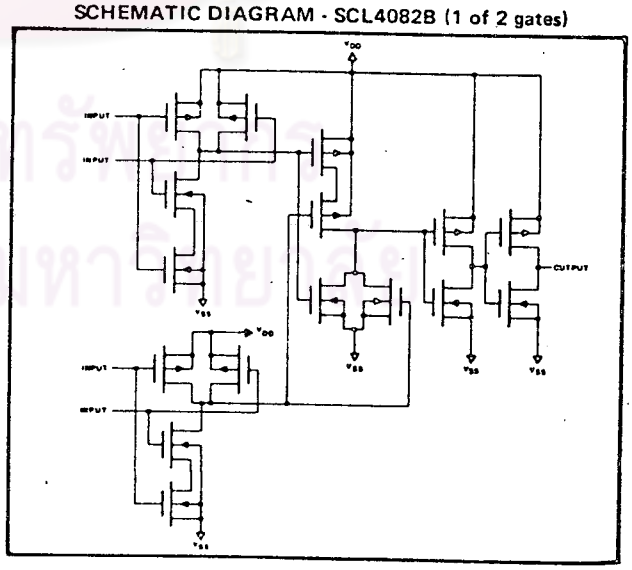


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM - SCL4082B (1 of 2 gates)



MM54C00/MM74C00 quad two-input NAND gate
MM54C02/MM74C02 quad two-input NOR gate
MM54C04/MM74C04 hex inverter
MM54C10/MM74C10 triple three-input NAND gate
MM54C20/MM74C20 dual four-input NAND gate

general description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

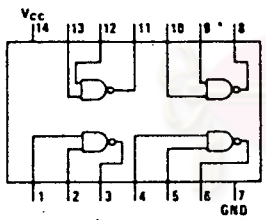
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power consumption	10 nW/package typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

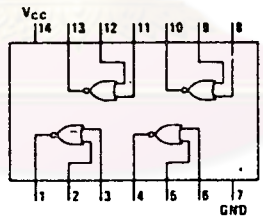
connection diagrams

MM54C00/MM74C00



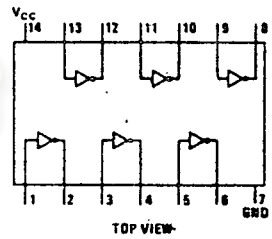
TOP VIEW

MM54C02/MM74C02



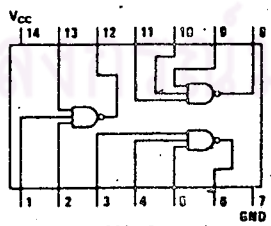
TOP VIEW

MM54C04/MM74C04



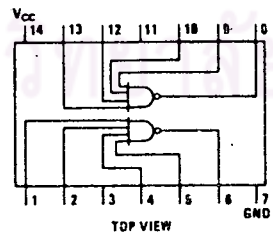
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

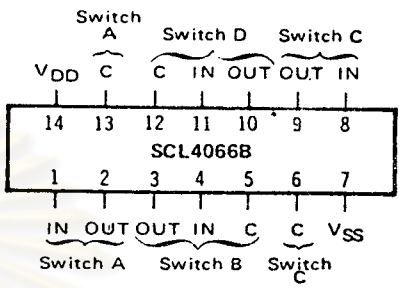
SCL4066B

CMOS QUAD ANALOG SWITCH

FEATURES

- Transmission or Multiplexing of Analog or Digital Signals
- 80Ω Typical ON-Resistance for 15-Volt operation
- Switch ON-Resistance Matched to within 5Ω over 15-Volt Signal-Input Range
- ON-Resistance Flat over Full Peak-to-Peak Signal Range
- High Degree of Linearity:
  ≤0.5% Distortion (typ) @ f_{is} = 1kHz,
  V_{is} = $5V_{p-p}$, V_{DD}-V_{SS} ≥ 10V, R_L = 10kΩ
- Extremely Low OFF switch Leakage Resulting in very Low Offset Current and High Effective OFF Resistance:
  10pA (typ) @ V_{DD}-V_{SS} = 10V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit):
  10^{12} Ω (typ)
- Low Crosstalk between Switches:
  -50dB (typ) @ f_{is} = 0.9MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitance Reduces Output Signal Transients
- Frequency Response, Switch ON = 40MHz (typ)

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

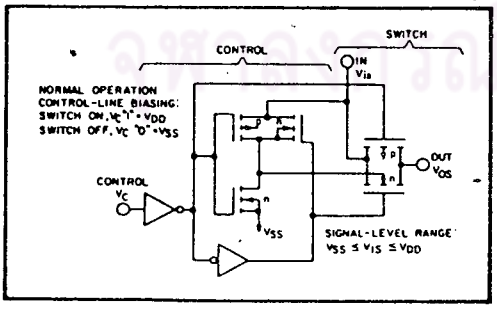
DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

DESCRIPTION

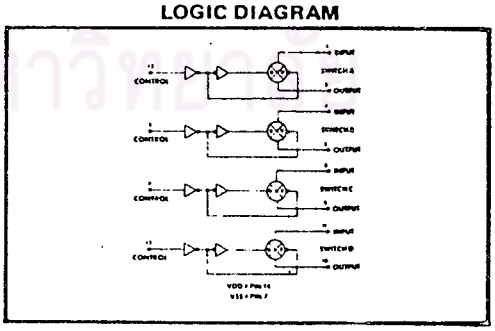
The SCL4066B is a Quad Bilateral Switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the SCL4016B, but exhibits a much lower ON-resistance. In addition, the ON-resistance is relatively constant over the full input signal range. The SCL4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the P and the N device in a given switch are biased ON or OFF simultaneously by the control signal. As shown below, the well of the N-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold voltage with input-signal, and thus keeps the ON-resistance low over the full operating range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON-impedance over the input-signal range. For sample-and-hold applications, however, the SCL4016 is recommended.

SCHEMATIC DIAGRAM (one of four switches)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1,3]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2]		25°C			T_{HIGH}[2]		Units
					Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD}	0	5	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		All valid input	0	10	–	0.1	–	0.001	0.1	–	3.0	
		combinations	0	15	–	0.2	–	0.002	0.2	–	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}	$V_{IS} = V_{SS}$	0	5	–	4.0	–	2.75	4.0	–	4.0	Vdc
		$V_{OS} = V_{DD}$	0	10	–	8.0	–	5.5	8.0	–	8.0	
		$I_{OS} = 10\mu A$	0	15	–	12.0	–	8.25	12.0	–	12.0	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	$V_{IS} = V_{SS}$	0	5	1.0	–	1.0	2.25	–	1.0	–	Vdc
		$V_{OS} = V_{DD}$	0	10	2.0	–	2.0	4.5	–	2.0	–	
		$I_{OS} = 10\mu A$	0	15	3.0	–	3.0	6.75	–	3.0	–	
SWITCH INPUT/OUTPUT LEAKAGE	I_{OFF}	$V_C = V_{SS}$	-7.5	+7.5	–	±100	–	±0.01	±100	–	±200	nAdc
		$V_{IS} = \pm 7.5$Vdc										
ON-RESISTANCE C,D,F,H device	R_{ON}	$V_C = V_{DD}$	-7.5	+7.5	–	220	–	80	280	–	320	Ω
		$V_{SS} \leq V_{IS} \leq V_{DD}$	0	+15								
		$R_L = 10k\Omega$	-5	+5	–	310	–	120	400	–	550	Ω
			0	+10								
			-2.5	+2.5	–	2000	–	270	2500	–	3500	Ω
			0	+5								
E device	R_{ON}	$V_C = V_{DD}$	-7.5	+7.5	–	250	–	80	280	–	300	Ω
		$V_{SS} \leq V_{IS} \leq V_{DD}$	0	+15								
		$R_L = 10k\Omega$	-5	+5	–	330	–	120	400	–	520	Ω
			0	+10								
			-2.5	+2.5	–	2100	–	270	2500	–	3200	Ω
			0	+5								
ON-RESISTANCE MATCH (Same package)	ΔR_{ON}	$V_C = V_{DD}$	-7.5	+7.5	–	–	–	5	–	–	–	Ω
		$V_{SS} \leq V_{IS} \leq V_{DD}$	0	+15								
		$R_L = 10k\Omega$	-5	+5	–	–	–	10	–	–		Ω
			0	+10								
			-2.5	+2.5	–	–	–	10	–	–		Ω
			0	+5								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications"

[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

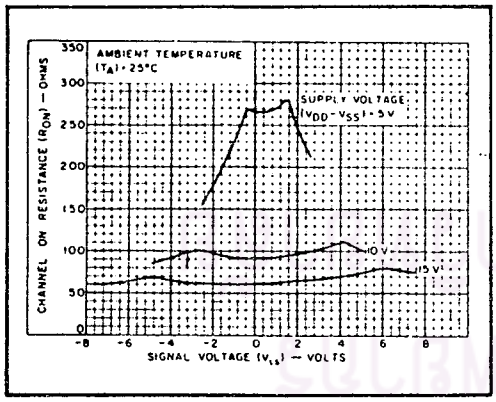
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

SCL4066B

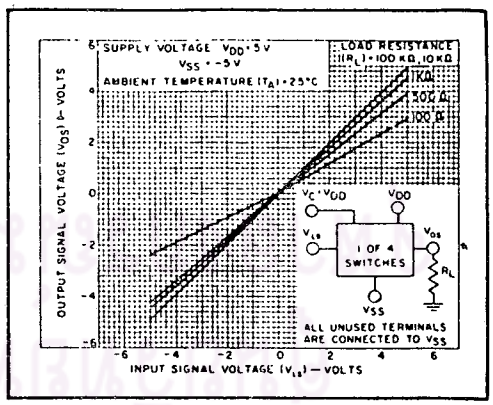
ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

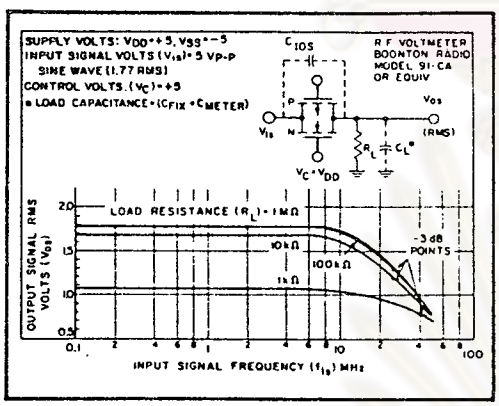
PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})								
PROPAGATION DELAY TIME Signal Input to Signal Output	t_{PLH}, t_{PHL}	V_c=V_{DD} V_{is}=Square Wave R_L = 10kΩ	0 0 0	5 10 15	– – –	20 10 7.5	40 20 15	ns
BANDWIDTH (-3dB) (Sine Wave)	BW	V_c=V_{DD} R_L V_{is}=5V_{p-p} 1kΩ centered 10kΩ @ 0.0Vdc 100kΩ 1MΩ	-5	+5	– – – –	54 40 38 37	– – – –	MHz
INSERTION LOSS (=20 $\log_{10}\frac{V_{os}}{V_{is}}$)		V_c=V_{DD} R_L V_{is}=5V_{p-p} 1kΩ centered 10kΩ @ 0.0Vdc 100kΩ 1MΩ	-5	+5	– – – –	2.3 0.2 0.1 0.05	– – – –	dB
SIGNAL DISTORTION (Sine Wave)		V_c=V_{DD} V_{is}=5V_{p-p} centered @ 0.0Vdc f_{is}=1.0kHz R_L = 10kΩ	-5	+5	–	0.16	–	%
FEEDTHROUGH (-50dB)		V_c=V_{SS} R_L V_{is}=5V_{p-p} 1kΩ centered 10kΩ @0.0Vdc 100kΩ 1MΩ	-5	+5	– – – –	1250 140 18 2	– – – –	kHz
CROSSTALK (-50dB) Between two switches		V_c(A)=V_{DD} V_c(B)=V_{SS} V_{is}(A)=5V_{p-p} centered @0.0Vdc R_L = 10kΩ	-5	+5	–	0.9	–	MHz
CAPACITANCE Input Output Feedthrough	C_{is} C_{os} C_{ios}	V_C = V_{SS}	-5	+5	– – –	8 8 0.5	– – –	pF pF pF
CONTROL INPUT (V_C)								
PROPAGATION DELAY TIME Turn on	t_{PC}	V_{SS}≤V_{is}≤V_{DD} R_L = 10kΩ	0 0 0	5 10 15	– – –	50 25 20	100 50 40	ns
MAXIMUM INPUT FREQUENCY	f_c	V_{SS}≤V_{is}≤V_{DD} R_L = 1.0kΩ	0 0 0	5 10 15	– – –	5 10 12	– – –	MHz
CROSSTALK (To signal port)		V_c=Square Wave R_L = 10kΩ R_{in} = 1.0kΩ	0 0 0	5 10 15	– – –	30 50 100	– – –	mV



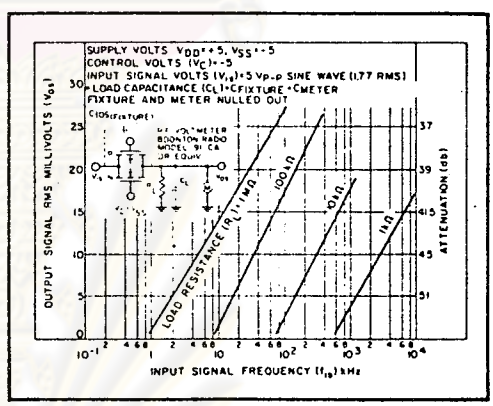
Typical channel ON resistance vs. signal voltage for three values of supply voltage (V_{DD}-V_{SS})



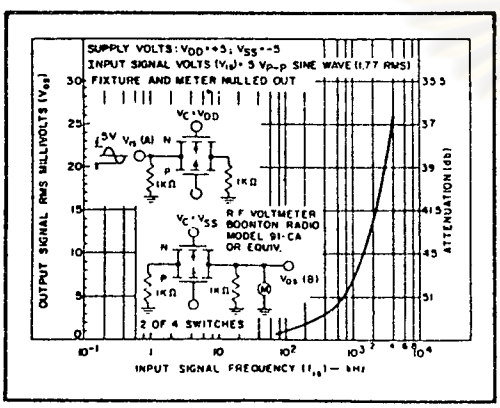
Typical ON characteristics for 1 of 4 channels.



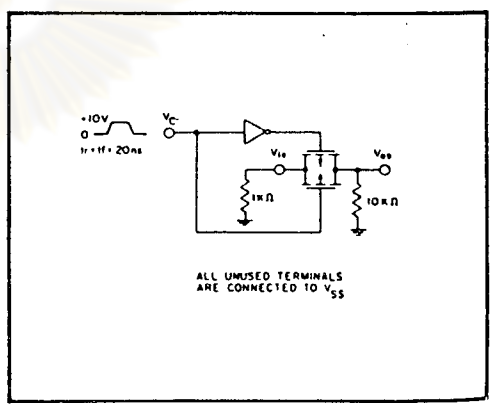
Typ. switch frequency response - switch "ON"



Typ. feedthru vs. freq. — switch "OFF"



Typ. crosstalk between switch circuits in the same package

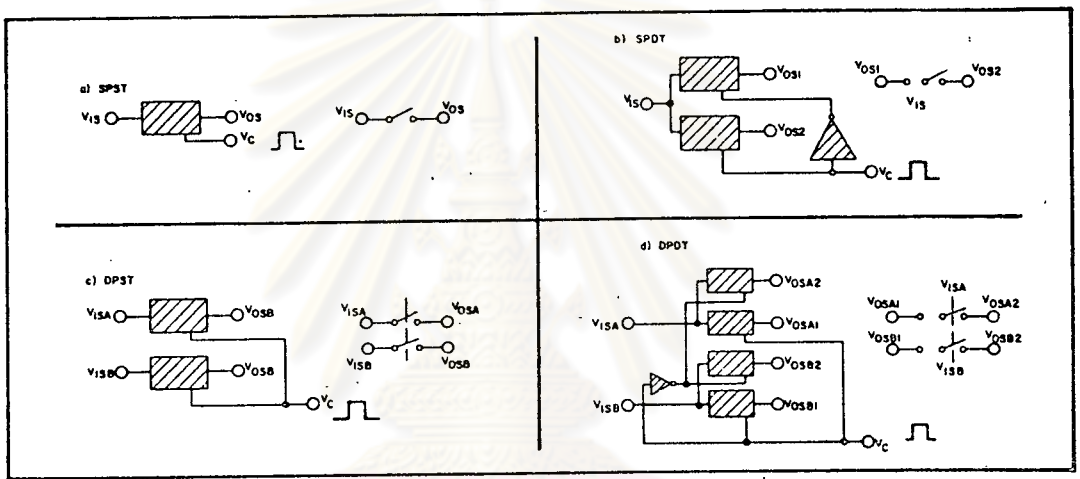


Test circuit, crosstalk-control input to signal output

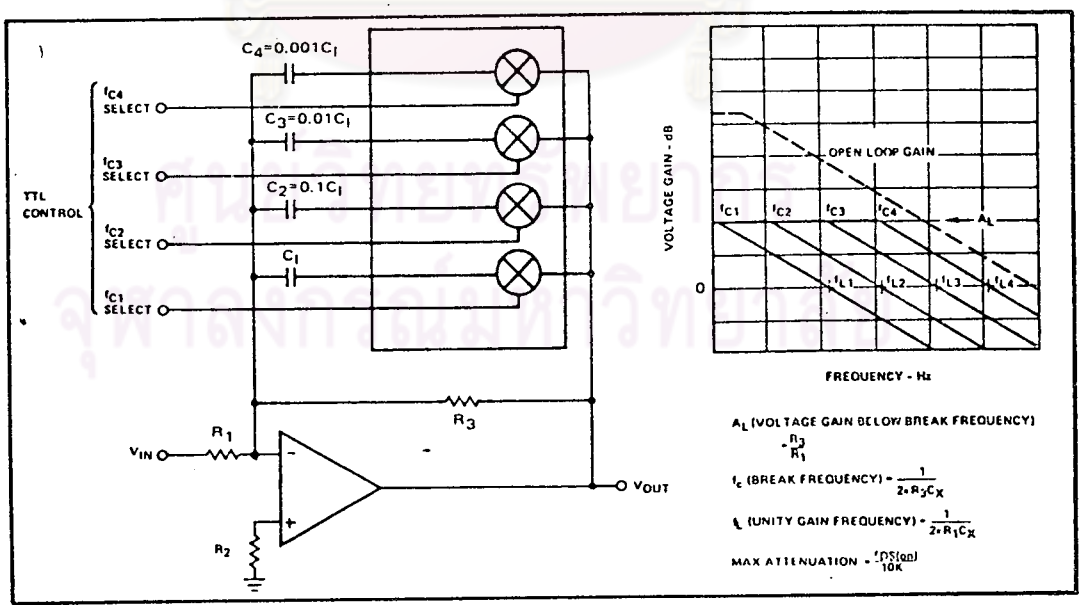
SPECIAL CONSIDERATIONS – SCL4066B

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 SCL4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from SCL4066B.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the sigoal.

APPLICATIONS INFORMATION



Basic Switch Functions using the SCL4066B



A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) $= -\frac{R_3}{R_1}$

f_c (BREAK FREQUENCY) $= \frac{1}{2\pi R_3 C_X}$

f_1 (UNITY GAIN FREQUENCY) $= \frac{1}{2\pi R_1 C_X}$

MAX ATTENUATION $= \frac{r_{DS(on)}}{10K}$

Active Low Pass Filter with Digitally Selected Break Frequency

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
54C	−55°C to +125°C
74C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Operating V_{CC} Range	3.0V to 15V
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
LOW POWER TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −10μA	4.4			V
	74C, V_{CC} = 4.75V, I_O = −10μA	4.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +10μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +10μA			0.4	V
CMOS TO LOW POWER					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	4.0			V
	74C, V_{CC} = 4.75V	4.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			1.0	V
	74C, V_{CC} = 4.75V			1.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	−1.75			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		50 30	90 60	ns ns
Input Capacitance (C_{IN})	(Note 2)		6.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		60 35	100 70	ns ns
Input Capacitance (C_{IN})	(Note 2)		7.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		18		pF
MM54C20/MM74C20					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		70 40	115 80	ns ns
Input Capacitance (C_{IN})	(Note 2)		9		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		30		pF

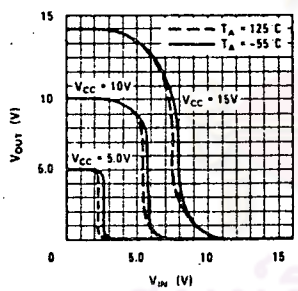
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

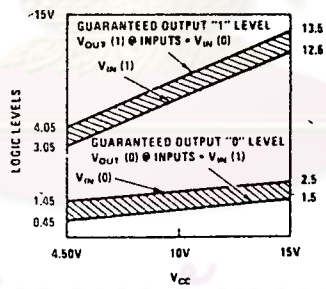
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90

typical performance characteristics

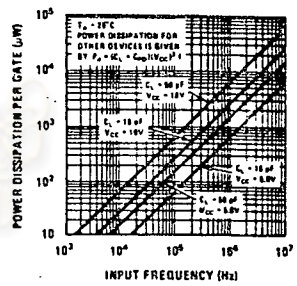
Gate Transfer Characteristics



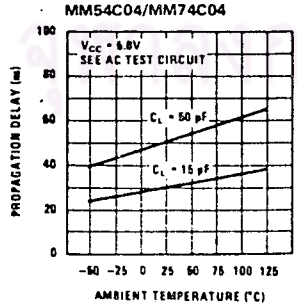
Guaranteed Noise Margin Over Temperature vs V_{CC}



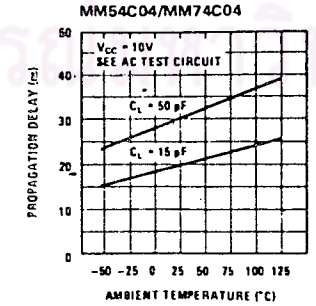
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



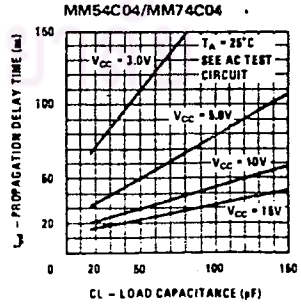
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

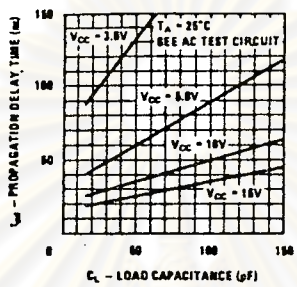


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

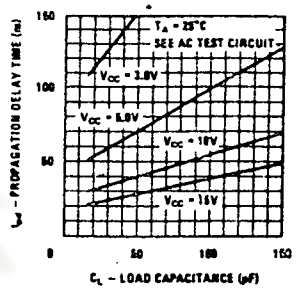


typical performance characteristics (con't)

Propagation Delay Time vs
Load Capacitance
MM54C10/MM74C10

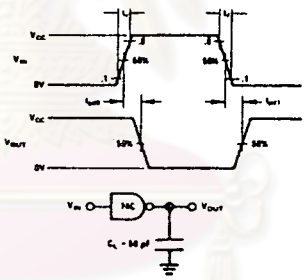


Propagation Delay Time vs
Load Capacitance
MM54C20/MM74C20



switching time waveforms and ac test circuits

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT $t_r, t_f \leq 20$ ns.

ภาคผนวก ข. ข้อมูลจำเพาะของเทอร์มิสเตอร์.

YSI PRECISION THERMISTOR

1444

YSI 44005

RESISTANCE 3000 OHMS @25°C

Interchangeability: ±0.2°C (See Tolerance Curves).

Max. Operating Temp: 150°C (300°F).

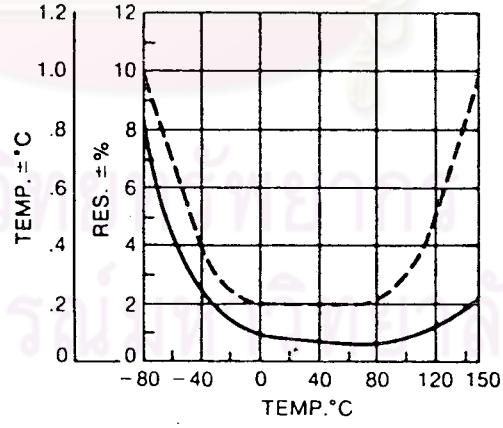
Time Constant, Max: 1 sec. in well stirred oil, 10 sec. in still air. Time constant is the time required for a thermistor to indicate 63% of a newly impressed temperature.

Dissipation Constant, Min: 8mW/°C in well stirred oil, 1mW/°C in still air. Dissipation constant is the power in milliwatts to raise a thermistor 1°C above surrounding temperature.

Color Code: Black epoxy body, green end.

Storage Temperature: -80° to +120°C (-112° to +250°F).

Tolerance Curves: The following curves indicate conformance to standard resistance temperature values as a % of resistance, and as a maximum interchangeability error expressed as temperature.



WARNING

Use heat sinks when soldering or welding to thermistor leads.

Industrial Division
Yellow Springs Instrument Co.
Yellow Springs, Ohio 45387, U.S.A.
Phone 513-767-7241
YSI

ITEM 003230 P/N B44505-F Printed in U.S.A. M.P.

RESISTANCE VERSUS TEMPERATURE —80° to +150°C

TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES
—80	2211K	—50	201.1K	—20	29.13K	+ 10	5971	+ 40	1598	+ 70	525.4	+100	203.8	+130	90.2
79	2022K	49	187.3K	19	27.49K	11	5692	41	1535	71	507.8	101	197.9	131	87.9
78	1851K	48	174.5K	18	25.95K	12	5427	42	1475	72	490.9	102	192.2	132	85.7
77	1696K	47	162.7K	17	24.51K	13	5177	43	1418	73	474.7	103	186.8	133	83.6
76	1555K	46	151.7K	16	23.16K	14	4939	44	1363	74	459.0	104	181.5	134	81.6
75	1426K	45	141.6K	15	21.89K	15	4714	45	1310	75	444.0	105	176.4	135	79.6
74	1309K	44	132.2K	14	20.70K	16	4500	46	1260	76	429.5	106	171.4	136	77.6
73	1202K	43	123.5K	13	19.58K	17	4297	47	1212	77	415.6	107	166.7	137	75.8
72	1105K	42	115.4K	12	18.52K	18	4105	48	1167	78	402.2	108	162.0	138	73.9
71	1016K	41	107.9K	11	17.53K	19	3922	49	1123	79	389.3	109	157.8	139	72.2
—70	935.4K	—40	101.0K	—10	16.60K	+ 20	3748	+ 50	1081	+ 80	376.9	+110	153.2	+140	70.4
69	861.4K	39	94.48K	9	15.72K	21	3583	51	1040	81	364.9	111	149.0	141	68.8
68	793.7K	38	88.46K	8	14.90K	22	3426	52	1002	82	353.4	112	145.0	142	67.1
67	731.8K	37	82.87K	7	14.12K	23	3277	53	965.0	83	342.2	113	141.1	143	65.5
66	675.2K	36	77.66K	6	13.39K	24	3135	54	929.6	84	331.5	114	137.2	144	64.0
65	623.3K	35	72.81K	5	12.70K	25	3000	55	895.8	85	321.2	115	133.6	145	62.5
64	575.7K	34	68.30K	4	12.05K	26	2872	56	863.3	86	311.3	116	130.0	146	61.1
63	532.1K	33	64.09K	3	11.44K	27	2750	57	832.2	87	301.7	117	126.5	147	59.6
62	492.1K	32	60.17K	2	10.86K	28	2633	58	802.3	88	292.4	118	123.2	148	58.3
61	455.3K	31	56.51K	— 1	10.31K	29	2523	59	773.7	89	283.5	119	119.9	149	56.8
—60	421.5K	—30	53.10K	0	9796	+ 30	2417	+60	746.3	+90	274.9	+120	116.8	+150	55.6
59	390.5K	29	49.91K	+ 1	9310	31	2317	61	719.9	91	266.6	121	113.8		
58	361.9K	28	46.94K	2	8851	32	2221	62	694.7	92	258.6	122	110.8		
57	335.7K	27	44.16K	3	8417	33	2130	63	670.4	93	250.9	123	107.9		
56	311.5K	26	41.56K	4	8006	34	2042	64	647.1	94	243.4	124	105.2		
55	289.2K	25	39.13K	5	7618	35	1959	65	624.7	95	236.2	125	102.5		
54	268.6K	24	36.86K	6	7252	36	1880	66	603.3	96	229.3	126	99.9		
53	249.7K	23	34.73K	7	6905	37	1805	67	582.6	97	222.6	127	97.3		
52	232.2K	22	32.74K	8	6576	38	1733	68	562.8	98	216.1	128	94.9		
51	216.0K	21	30.87K	9	6265	39	1664	69	543.7	99	209.8	129	92.5		

ภาคผนวก ก. ADC

National Semiconductor

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

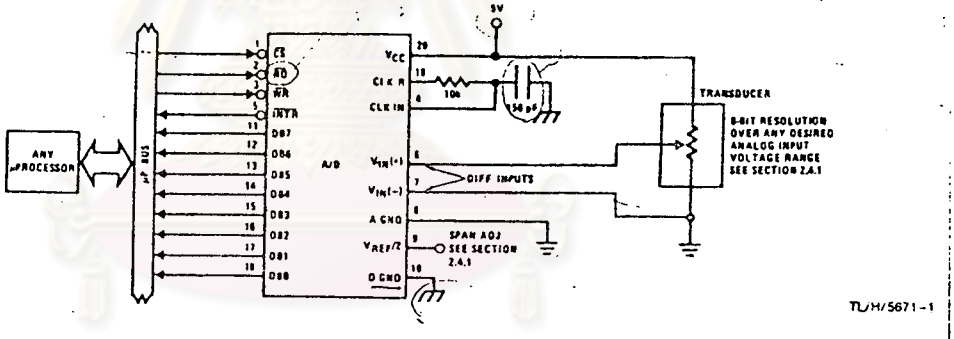
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

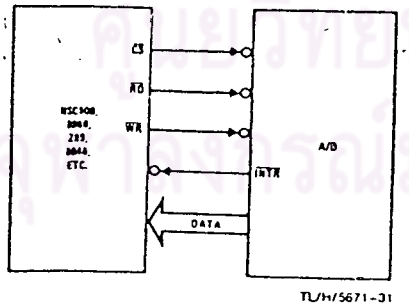
- Resolution — 8 bits
- Total error — ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time — 100 μs

Typical Applications



TL/H/5671-1

8080 Interface



TL/H/5671-31

Part Number	Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)		
	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	0°C ≤ T_A ≤ +70°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± ½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± 1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			± 1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 1.0	8.0 1.3		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd-0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		± 1/16	± ⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ± 10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		± 1/16	± ⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			0.4 0.4	V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = "1" ADC0801/02/03/05 ADC0804 (Note 9)		1.1 1.9	1.8 2.5	mA mA

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

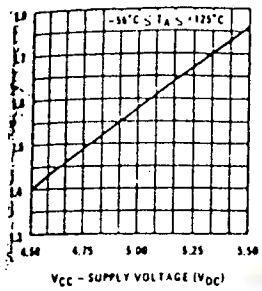
Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

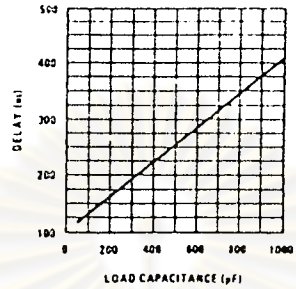
Note 9: For ADC0804LC nominal value of $V_{REF}/2$ is ...

Typical Performance Characteristics

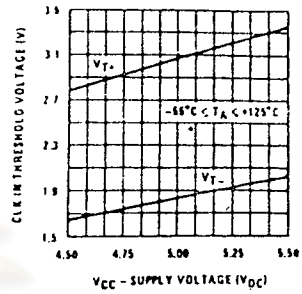
Logic Input Threshold Voltage vs. Supply Voltage



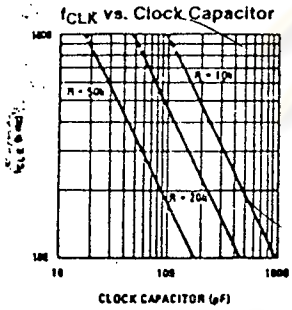
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



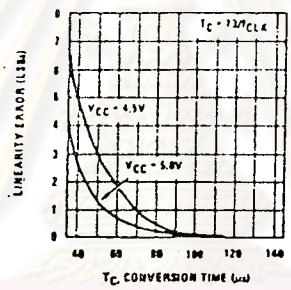
CLK IN Schmitt Trip Levels vs. Supply Voltage



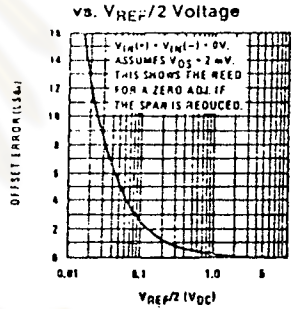
f_{CLK} vs. Clock Capacitor



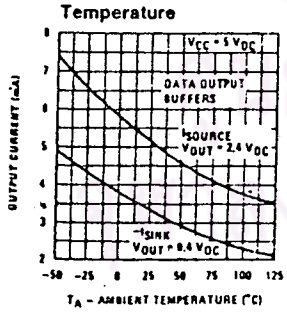
Full-Scale Error vs Conversion Time



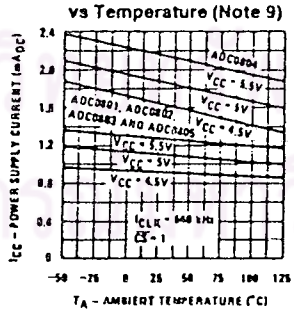
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



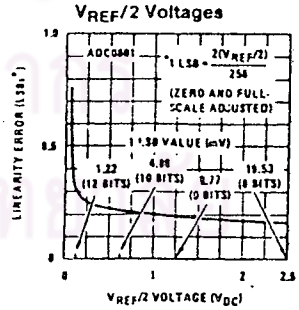
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



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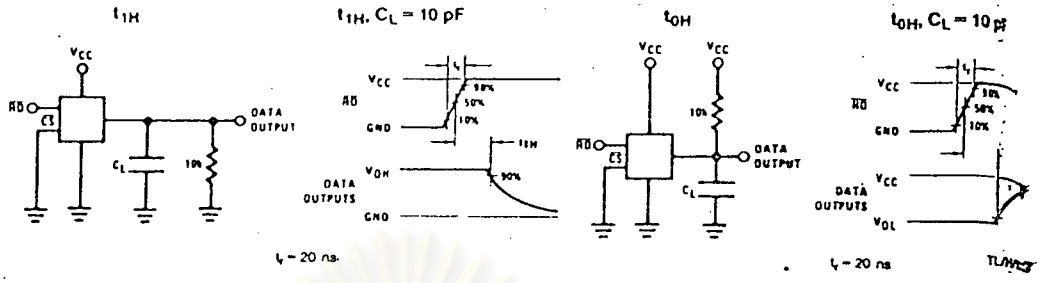
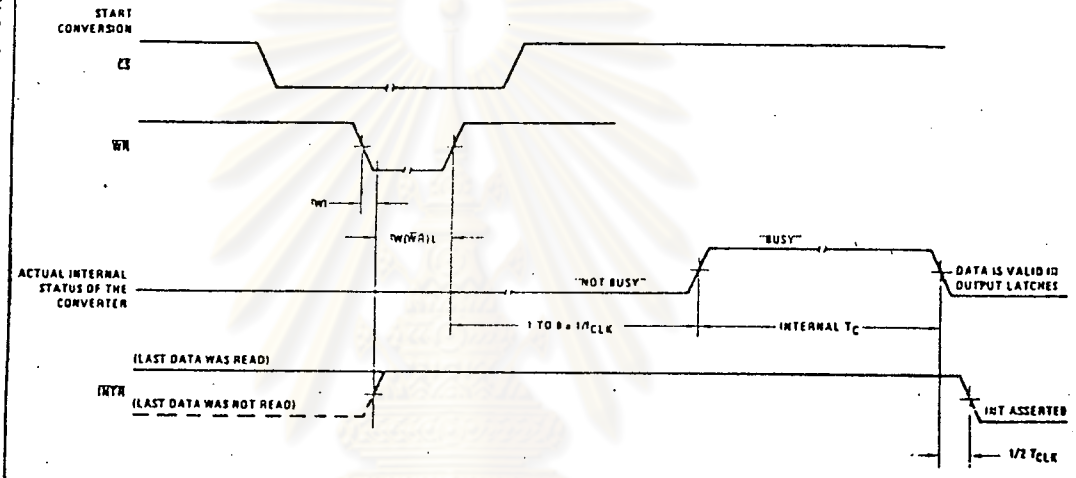
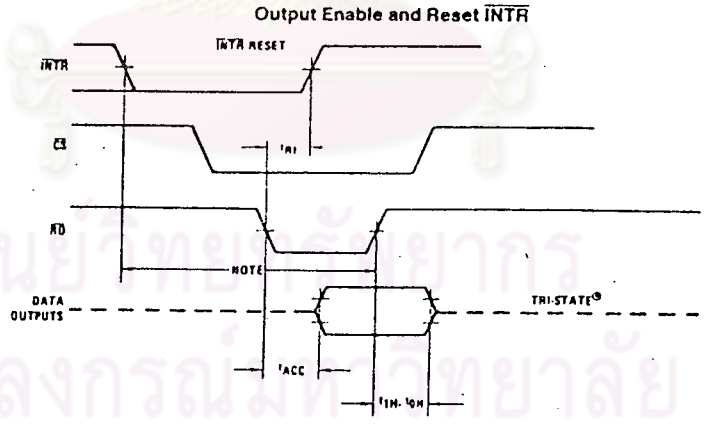
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$



Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

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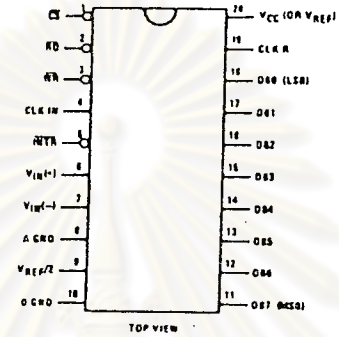
Ordering Information

TEMPERATURE RANGE		0°C TO 70°C	−40°C TO +85°C	−40°C TO +85°C	−55°C TO +125°C
ERROR	± ¼ Bit Adjusted		ADC0801LCN	ADC0801LCJ	ADC0801LJ
	± ½ Bit Unadjusted		ADC0802LCN	ADC0802LCJ	ADC0802LJ
	± ½ Bit Adjusted		ADC0803LCN	ADC0803LCJ	
	± 1Bit Unadjusted	ADC0804LCN	ADC0805LCN	ADC0804LCJ	
PACKAGE OUTLINE		N20A-MOLDED DIP		J20A-CAVITY DIP	J20A-CAVITY DIP

Connection Diagram

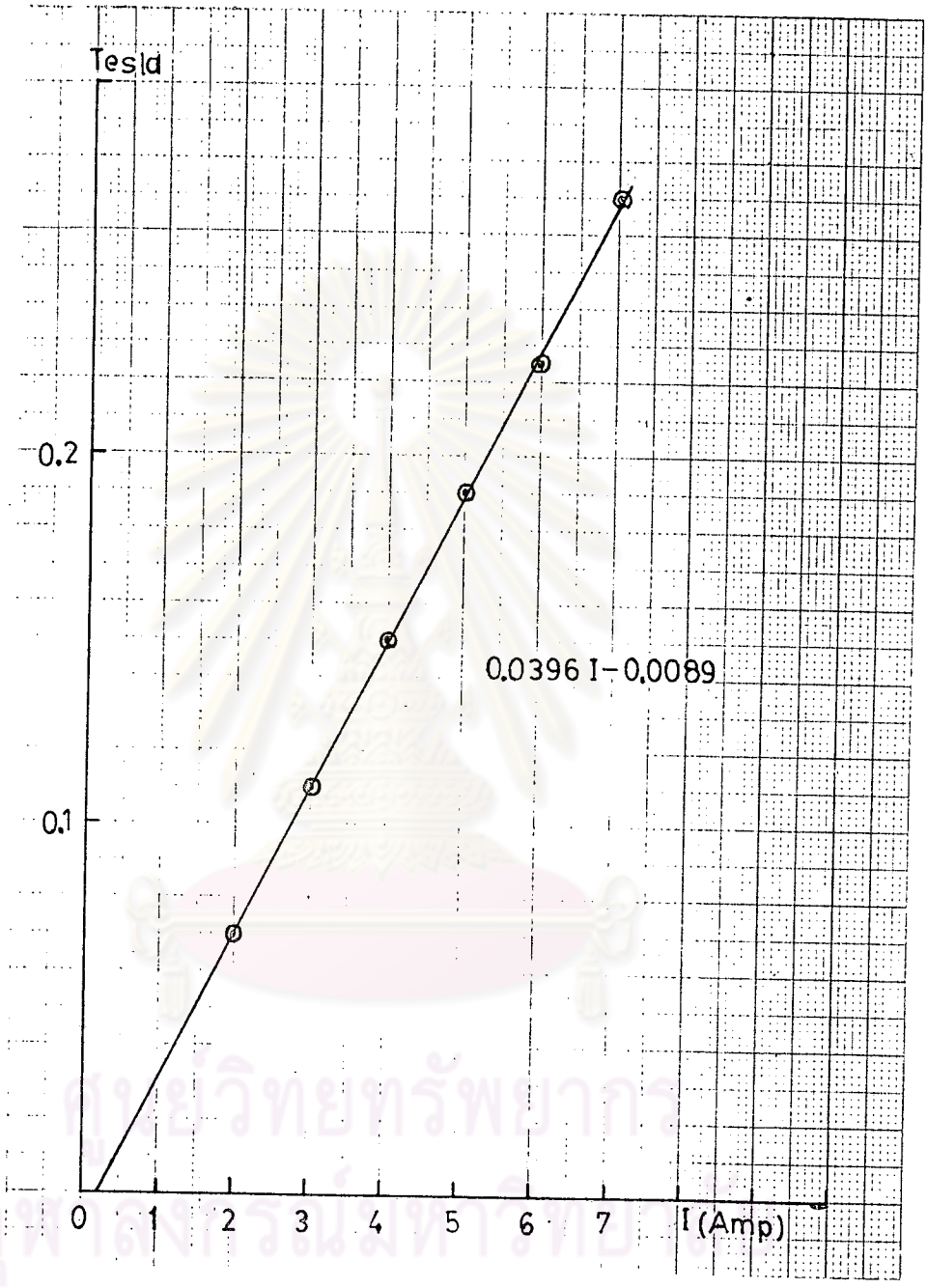
ADC080X
Dual-In-Line Package



TL/H/5671-30

See Ordering Information

ภาคผนวก ง ความสัมพันธ์ระหว่างสนามแม่เหล็กกับกระแส



ภาคผนวก จ.

สัญญลักษณ์

สัญญลักษณ์	ความหมาย
ρ	สภาพต้านทานไฟฟ้า
R_H	สัมประสิทธิ์ของฮอลล์
μ_H	สภาพความเคลื่อนได้
$T(^{\circ}C)$	อุณหภูมิในหน่วยเซลเซียส
$T(K)$	อุณหภูมิสัมบูรณ์
n	ความหนาแน่นพาหะ

ประวัติผู้เขียน

นายมนู เฟื่องฟุ้ง เกิดวันที่ 11 สิงหาคม พ.ศ. 2502 จังหวัดนครนายก ได้รับปริญญาวิทยาศาสตรบัณฑิตสาขาฟิสิกส์ จากคณะวิทยาศาสตร์ มหาวิทยาลัยรามคำแหง เมื่อ พ.ศ.2525 จากนั้นได้เข้าศึกษาต่อในระดับปริญญาโทบัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ. 2526