# รายการอ้างอิง

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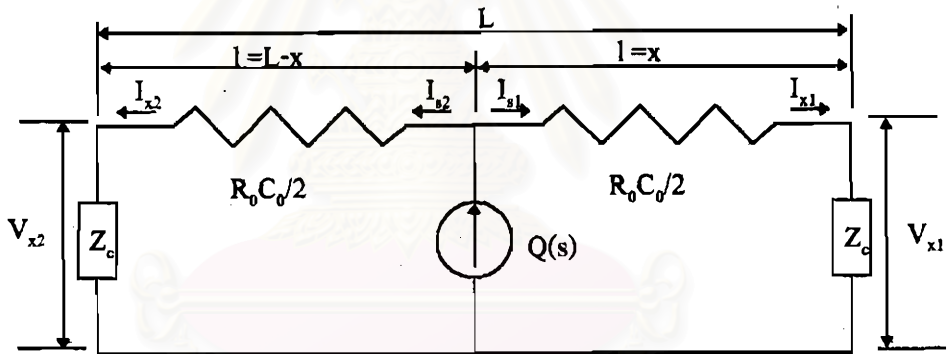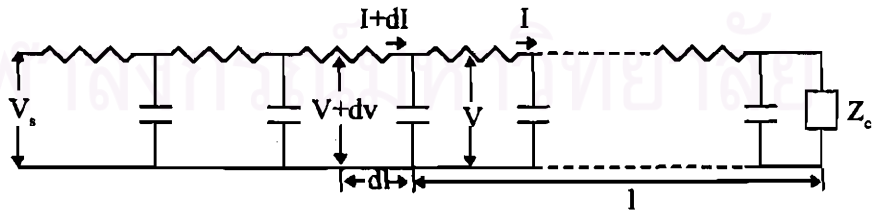   39(1968).

ภาคผนวก
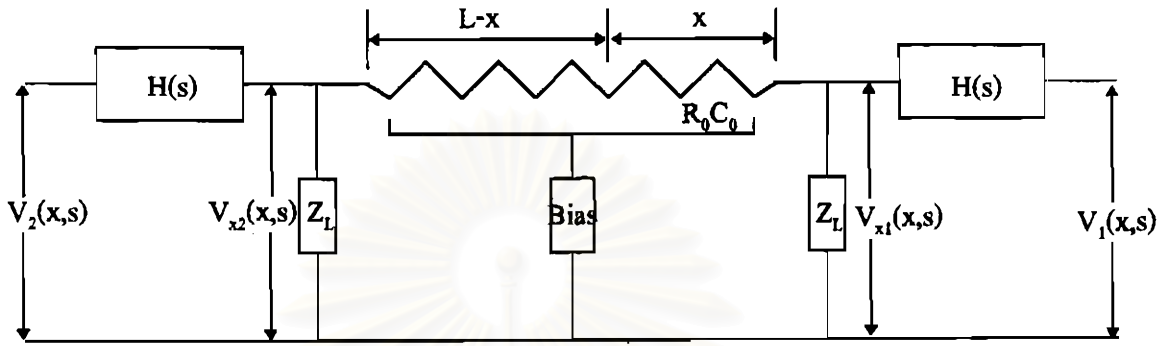
รูปที่ 1 วงจรสมมูลย์ทางไฟฟ้าของหัววัดรังสีชนิดไวต่อตำแหน่ง

รูปที่ 2 วงจรสมมูลย์ของหัววัดขณะวัดรังสี

รูปที่ 3 สมมูลย์ของวงจรในรูปแบบสายส่งแสดงการเคลื่อนของสัญญาณสู่โหลด

จากรูปที่ 3 จากกฎของ KCL จะได้

$$dV = \frac{(I + dI) + (I)}{2} . zdl$$

$$dV = Izdl + \frac{dI}{2} . zdl \qquad \ldots\ldots\ldots\ldots(1)$$

เทอมของ $\qquad \frac{dI}{2} . zdl \qquad$ มีค่าน้อยมากๆจึงคิดเทียบเท่ากับ 0

ในทำนองเดียวกันจากกฎของ KVL จะได้

$$dI = \frac{(V + dV) + (V)}{2} . ydl$$

$$dI = Vydl + \frac{dV}{2} . ydl \qquad \ldots\ldots\ldots\ldots(2)$$

เทอมของ $\qquad \frac{dV}{2} . ydl \qquad$ มีค่าน้อยมากๆจึงคิดเทียบเท่ากับ 0

จากสมการที่ 1 $\qquad \dfrac{dV}{dl} = Iz \qquad \qquad \ldots\ldots\ldots\ldots(3)$

จากสมการที่ 2 $\qquad \dfrac{dI}{dl} = Vy \qquad \qquad \ldots\ldots\ldots\ldots(4)$

ดิฟเฟอเรนชิเอตสมการที่ 3 เทียบกับ l จะได้

$$\frac{d^2V}{dl^2} = \frac{zdI}{dl}$$

แทนค่า $\qquad \dfrac{dI}{dl} = Vy \qquad$ จะได้

$$\frac{d^2V}{dl^2} = yzV \qquad\qquad \dots\dots\dots(5)$$

แก้สมการที่ 5 ด้วย Differential Equations จะได้

$$V = A_1 e^{\sqrt{yz}l} + A_2 e^{-\sqrt{yz}l} \qquad\qquad \dots\dots\dots(6)$$

ให้ $\qquad n = \sqrt{R_0 S C_0} = \sqrt{yz} \qquad$ propagation constant

ถ้า $\qquad l = 0 \quad$ จะได้ $\quad V = V_{x1}$

$$V_{x1} = A_1 + A_2 \qquad\qquad \dots\dots\dots(7)$$

จากสมการที่ 3 $\qquad \dfrac{dV}{dl} = Iz$

$$I = \frac{1}{z}\frac{dV}{dl}$$

ดิฟเฟอเรนชิเอตสมการที่ 6 แล้วแทนค่าใน $\dfrac{dV}{dl}$

$$I = \frac{1}{z}\left(\sqrt{yz}A_1 e^{\sqrt{yz}l} - \sqrt{yz}A_2 e^{-\sqrt{yz}l}\right)$$

$$= \frac{1}{\sqrt{z/y}}\left[A_1 e^{\sqrt{yz}l} - A_2 e^{-\sqrt{yz}l}\right]$$

$$= \frac{1}{Z_0}\left[A_1 e^{\sqrt{yz}l} - A_2 e^{-\sqrt{yz}l}\right]$$

กำหนดให้ $\qquad Z_0 = \sqrt{R_0 \Big/ SC_0} \ $ = Characteristic Impedance

ทำนองเดียวกันถ้า $\qquad l = 0$ จะได้ $\quad I = I_{x1}$

$$I_{x1} = \frac{1}{Z_0}\left(A_1 - A_2\right) \qquad\qquad \ldots\ldots\ldots\ldots(8)$$

แก้สมการที่ 7 และ 8 หาค่า A_1 และ A_2

$$V_{x1} + Z_0 I_{x1} = 2A_1$$

$$A_1 = \frac{V_{x1} + Z_0 I_{x1}}{2} \qquad\qquad \ldots\ldots\ldots\ldots(9)$$

เอาสมการที่ 7 ลบสมการที่ 8 จะได้

$$V_{x1} - Z_0 I_{x1} = 2A_2$$

$$A_2 = \frac{V_{x1} - Z_0 I_{x1}}{2} \qquad\qquad \ldots\ldots\ldots\ldots(10)$$

จากวงจรรูปที่ 1 $\qquad V_{x1} = Z_c I_{x1}$

$$I_{x1} = \frac{V_{x1}}{Z_c}$$

เอาค่า $\qquad I_{x1} = \dfrac{V_{x1}}{Z_c} \qquad$ แทนในสมการที่ 9 และ 10

จะได้ $\qquad A_1 = \dfrac{V_{x1} + \dfrac{Z_0}{Z_c}V_{x1}}{2} \qquad\qquad \ldots\ldots\ldots\ldots(11)$

$$A_2 = \frac{V_{x1} - \dfrac{Z_0}{Z_c}V_{x1}}{2} \qquad\qquad \ldots\ldots\ldots\ldots(12)$$

แทนค่า A_1 และ A_2 ในสมการที่ 6

$$V = \left[\frac{V_{x1} + \frac{Z_0}{Z_c}V_{x1}}{2}\right]e^{nl} + \left[\frac{V_{x1} - \frac{Z_0}{Z_c}V_{x1}}{2}\right]e^{-nl}$$

$$= V_{x1}\left[\frac{e^{nl} + e^{-nl}}{2}\right] + \frac{Z_0}{Z_c}V_{x1}\left[\frac{e^{nl} - e^{-nl}}{2}\right]$$

จาก $\quad \cosh nl = \dfrac{e^{nl} + e^{-nl}}{2} \quad$ และ $\quad \sinh nl = \dfrac{e^{nl} - e^{-nl}}{2}$

จัดรูปสมการจะได้

$$V = V_{x1}\cosh nl + \frac{Z_0}{Z_c}V_{x1}\sinh nl \qquad \ldots\ldots\ldots(13)$$

ในทำนองเดียวกัน

$$Z_0 I = A_1 e^{nl} - A_2 e^{-nl}$$

$$Z_0 I = \left[\frac{V_{x1} + \frac{Z_0}{Z_c}V_{x1}}{2}\right]e^{nl} - \left[\frac{V_{x1} - \frac{Z_0}{Z_c}V_{x1}}{2}\right]e^{-nl}$$

$$= V_{x1}\left[\frac{e^{nl} - e^{-nl}}{2}\right] + \frac{Z_0}{Z_c}V_{x1}\left[\frac{e^{nl} + e^{-nl}}{2}\right]$$

จัดรูปสมการจะได้

$$Z_0 I = V_{x1}\sinh nl + \frac{Z_0}{Z_c}V_{x1}\cosh nl \qquad \ldots\ldots\ldots(14)$$

ที่ระยะ $\qquad l = x \qquad$ จะได้ $\qquad V = V_s$

$$V_s = V_{x1}\cosh nx + \frac{Z_0}{Z_c}V_{x1}\sinh nx \qquad \ldots\ldots\ldots(15)$$

ที่ระยะ $\qquad l = L - x \qquad$ จะได้ $\qquad V = V_s$

$$V_s = Vx_2 \cosh n(L-x) + \frac{Z_0}{Z_c}V_{x2}\sinh n(L-x) \qquad \ldots\ldots\ldots(16)$$

สมการที่ 15 เท่ากับสมการที่ 16

$$V_{x1}\left[\cosh nx + \frac{Z_0}{Z_c}\sinh nx\right] = V_{x2}\left[\cosh n(L-x) + \frac{Z_0}{Z_c}\sinh nx\right] \qquad \ldots\ldots\ldots(17)$$

ที่ระยะ $\qquad l = x \qquad$ จะได้ $\qquad I = I_{s1}$

$$Z_0 I_{s1} = V_{x1}\sinh nx + \frac{Z_0}{Z_c}V_{x1}\cosh nx$$

$$I_{s1} = \frac{V_{x1}}{Z_0}\sinh nx + \frac{V_{x1}}{Z_c}\cosh nx$$

$$I_{s1} = Y_o V_{x1}\sinh nx + Y_c V_{x1}\cosh nx \qquad \ldots\ldots\ldots(18)$$

ที่ระยะ $\qquad l = L-x \quad$ จะได้ $\qquad I = I_{s2}$

$$I_{s2} = Y_0 V_{x2}\sinh n(L-x) + Y_c V_{x2}\cosh n(L-x) \qquad \ldots\ldots\ldots(19)$$

จากรูปที่ 2 $\qquad Q(s) = I_{s1} + I_{s2}$

เอาสมการที่ 18 บวก 19 $= Q(s)$

$$Q(s) = V_{x1}\left[Y_0\sinh nx + Y_c\cosh nx\right] + V_{x2}\left[Y_0\sinh n(L-x) + Y_c\cosh n(L-x)\right] \qquad \ldots\ldots\ldots(20)$$

จากสมการที่ 17

$$V_{x2} = V_{x1} \frac{\left[\cosh nx + \dfrac{Z_0}{Z_c}\sinh nx\right]}{\left[\cosh n(L-x) + \dfrac{Z_0}{Z_c}\sinh(L-x)\right]} \qquad \ldots\ldots\ldots(21)$$

เอาค่า V_{x2} จากสมการที่ 21 แทนในสมการที่ 20

$$Q(s) = V_{x1}\left[Y_0 \sinh nx + Y_c \cosh nx\right]$$

$$+ V_{x1}\frac{\left[\cosh nx + \dfrac{Z_0}{Z_c}\sinh nx\right]}{\left[\cosh n(L-x) + \dfrac{Z_0}{Z_c}\sinh n(L-x)\right]} * \left[Y_0 \sinh n(L-x) + Y_c \cosh n(L-x)\right]$$

เอาเทอมของ $\left[\cosh n(L-x) + \dfrac{Z_0}{Z_c}\sinh n(L-x)\right]$ คูณตลอดจะได้

$$Q(s)\left[\cosh n(L-x) + \frac{Z_0}{Z_c}\sinh n(L-x)\right] = V_{x1}\left[Y_0 \sinh nx + Y_c \cosh nx\right]\left[\cosh n(L-x) + Z_0 Y_c \sinh n(L-x)\right]$$

$$+ V_{x1}\left[\cosh nx + Z_0 Y_c \sinh nx\right]\left[Y_0 \sinh n(L-x) + Y_c \cosh n(L-x)\right]$$

$$Q(s)\left[\cosh n(L-x) + \frac{Z_0}{Z_c}\sinh n(L-x)\right] = V_{x1}\begin{bmatrix} Y_0 \sinh nx.\cosh n(L-x) + Y_c \sinh nx.\sinh n(L-x) \\ + Y_c \cosh nx.\cosh n(L-x) + Z_0 Y_c^2 \cosh nx.\sinh n(L-x) \\ + Y_0 \cosh nx.\sinh n(L-x) + Y_c \cosh nx.\cosh n(L-x) \\ + Y_c \sinh nx.\sinh n(L-x) + Z_0 Y_c^2 \sinh nx.\cosh n(L-x) \end{bmatrix}$$

จาก
$$\sinh(A+B) = \sinh A \cosh B + \cosh B \sinh A$$
$$\cosh(A+B) = \sinh A \sinh B + \cosh A \cosh B$$

จะได้

$$Q(s)\left[\cosh n(L-x) + \frac{Z_0}{Z_c}\sinh n(L-x)\right] = V_{x1}\begin{bmatrix} Y_0\left[\sinh(nx+n(L-x))\right] + Y_c\left[\cosh(nx+n(L-x))\right] \\ + Y_c\left[\cosh(nx+n(L-x))\right] + Z_0 Y_c^2\left[\sinh(nx+n(L-x))\right] \end{bmatrix}$$

$$Q(s)\left[\cosh n(L-x) + \frac{Z_0}{Z_c}\sinh n(L-x)\right] = V_{x1}\left[(Y_0 + Z_0 Y_c^2)\sinh nL + 2Y_c \cosh nL\right]$$

เอา $\quad Z_c \quad$ คูณทั้งสองข้างจะได้

$$Q(s)Z_c\left[\cosh n(L-x) + Z_0 Y_c \sinh n(L-x)\right] = V_{x1}\left[(Y_0 Z_c + Z_0 Y_c)\sinh nL + 2\cosh nL\right]$$

จะได้ค่า

$$V_{x1}(s,x) = Q(s)Z_c \frac{\cosh n(L-x) + Z_0 Y_c \sinh n(L-x)}{(Y_0 Z_c + Z_0 Y_c)\sinh nL + 2 \cosh nL} \qquad \ldots\ldots\ldots\ldots(22)$$

แทนค่า x ด้วย $L-x$ จะได้

$$V_{x2}(s,x) = Q(s)Z_c \frac{\cosh nx + Z_0 Y_c \sinh nx}{(Y_0 Z_c + Z_0 Y_c)\sinh nL + 2\cosh nL} \qquad \ldots\ldots\ldots\ldots(23)$$

ภาคผนวก ข.

LND 42423

LINEAR FLOW POSITION SENSITIVE

X-RAY DETECTOR

GENERAL SPECIFICATIONS

Path Length (inch/mm)	0.75 / 19.1
Cathode Material	Aluminum
Maximum Length (inch/mm)	8.38 / 212.9
Effective Length (inch/mm)	4.0 / 101.6
Maximum Width (inch/mm)	1.5 / 38.1
Effective Width (inch/mm)	0.59 / 15.0
Connector	Wire Lead
Maximum Operating Temperature $^{\circ}$C	50
Anode	8 KΩ/mm Pyrolytic Quartz

WINDOW SPECIFICATIONS

Material	Mylar
Areal Density (mg/cm^2)	9.2
Thickness (inch/mm)	0.0005 / 0.0127
Dimensions (inch/mm)	0.59/15.0 x 4.0/101.6

ELECTRICAL SPECIFICATIONS

Recommended Operating Voltage (volts)	Dependent on Gas
Typical Resolution (%FWHM Fe^{55})	18
Position Resolution (mm)	0.25

FLOW PORTS (2)

FLYING LEADS 3" LONG TYP
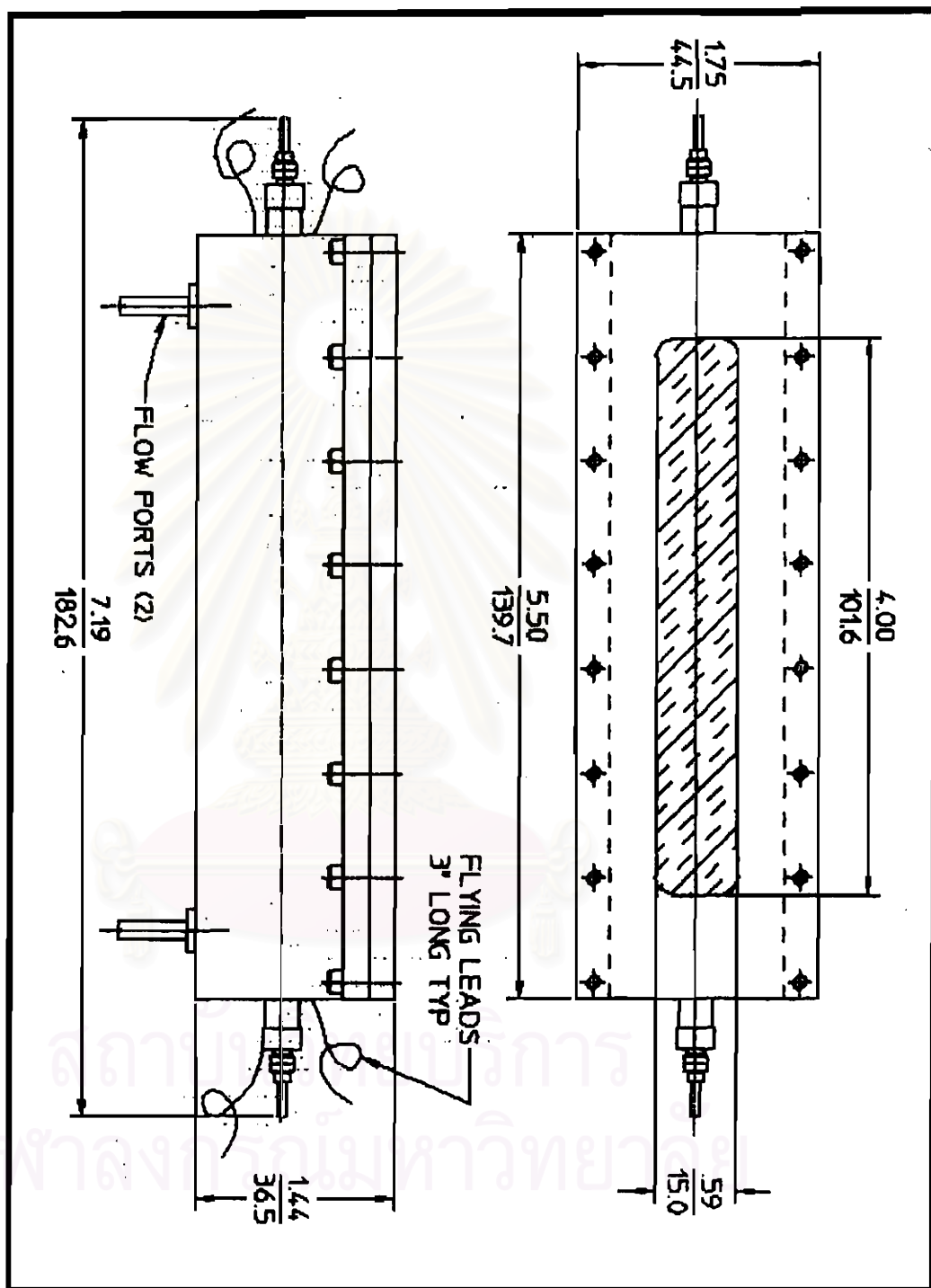
หมายเหตุ   ได้สอบถามราคาของ Linear flow position-sensitive x-ray detector Model LND 42423 ไปยังผู้ผลิตต่างประเทศมีราคา 3000 ดอลลาร์ ค่า U.P.S 110 ดอลลาร์

ภาคผนวก ก.

N *National Semiconductor*

March 1998

LM118/LM218/LM318
Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Connection Diagram

Dual-In-Line Package

DS007766-24
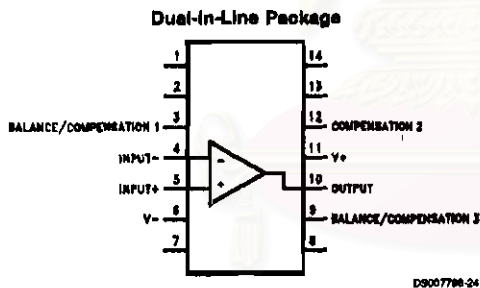
Top View
Order Number LM118J/883 (Note 2)
See NS Package Number J14A

Dual-In-Line Package

DS007766-3
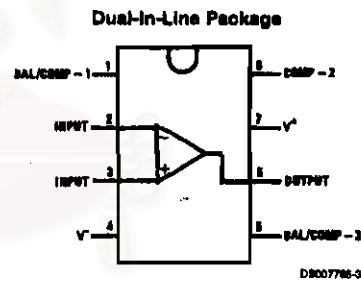
Top View
Order Number LM118J-8/883 (Note 2),
LM318M or LM318N
See NS Package Number J08A, M08A or N08B

Connection Diagram (Continued)

Metal Can Package
(Note 1)

DS007785-2
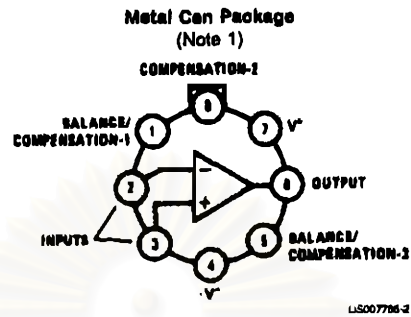
Top View
Order Number LM118H, LM118H/883 (Note 2),
LM218H or LM318H
See NS Package Number H08C

Note 1: Pin connections shown on schematic diagram and typical applications are for TO-5 package.
Note 2: Available per JM38510/10107.

Absolute Maximum Ratings (Note 8)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 3)	500 mW
Differential Input Current (Note 4)	±10 mA
Input Voltage (Note 5)	±15V
Output Short-Circuit Duration	Continuous

Operating Temperature Range

LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

Hermetic Package	300°C
Plastic Package	260°C

Soldering Information

Dual-In-Line Package

Soldering (10 sec.)	260°C

Small Outline Package

Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 9)	2000V

Electrical Characteristics (Note 6)

Parameter	Conditions	LM118/LM218			LM318			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2	4		4	10	mV
Input Offset Current	$T_A = 25°C$		6	50		30	200	nA
Input Bias Current	$T_A = 25°C$		120	250		150	500	nA
Input Resistance	$T_A = 25°C$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25°C$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L ≥ 2$ kΩ	50	200		25	200		V/mV
Slew Rate	$T_A = 25°C$, $V_S = ±15V$, $A_V = 1$ (Note 7)	50	70		50	70		V/µs
Small Signal Bandwidth	$T_A = 25°C$, $V_S = ±15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125°C$		4.5	7				mA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L ≥ 2$ kΩ	25			20			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 2$ kΩ	±12	±13		±12	±13		V
Input Voltage Range	$V_S = ±15V$	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 3: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 4: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 6: These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C (LM118), −25°C ≤ T_A ≤ +85°C (LM218), and 0°C ≤ T_A ≤ +70°C (LM318). Also, power supplies must be bypassed with 0.1 µF disc capacitors.

Note 7: Slew rate is tested with $V_S = ±15V$. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/µs.

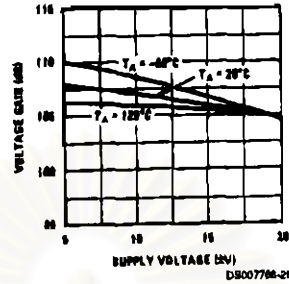**Note 8:** Refer to RETS118X for LM118H and LM118J military specifications.

Note 9: Human body model, 1.5 kΩ in series with 100 pF.

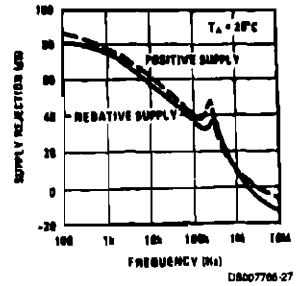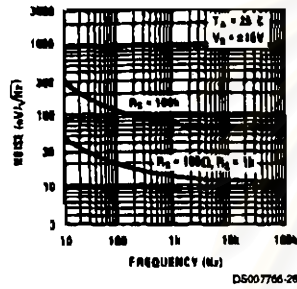# Typical Performance Characteristics LM118, LM218

Input Current
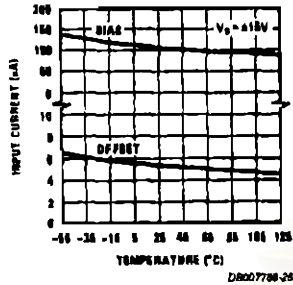
Voltage Gain
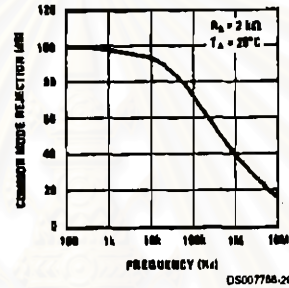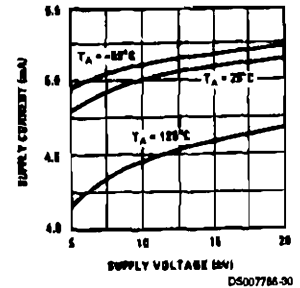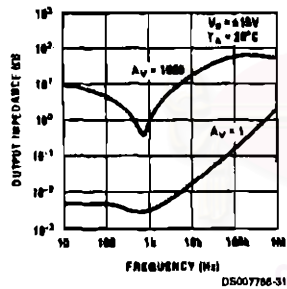
Power Supply Rejection

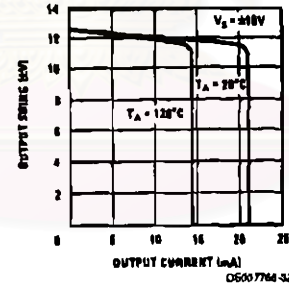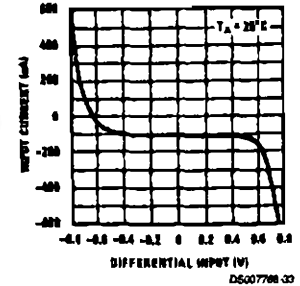**Input Noise Voltage**

Common Mode Rejection
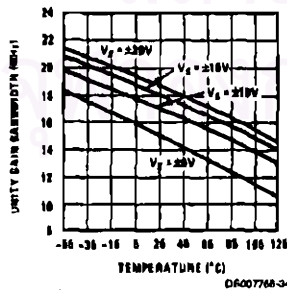
Supply Current
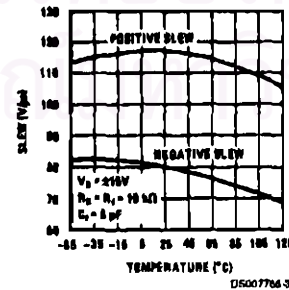
Closed Loop Output Impedance
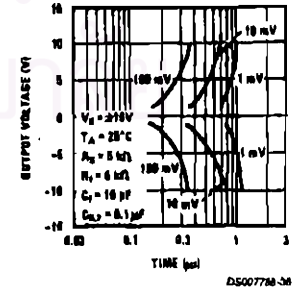
Current Limiting

Input Current

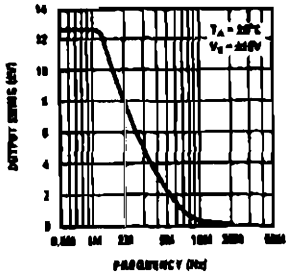**Unity Gain Bandwidth**

Voltage Follower Slew Rate

Inverter Settling Time

Typical Performance Characteristics LM118, LM218 (Continued)
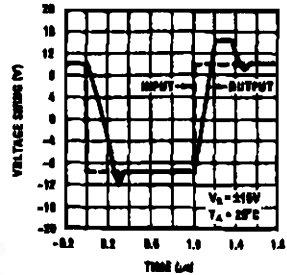
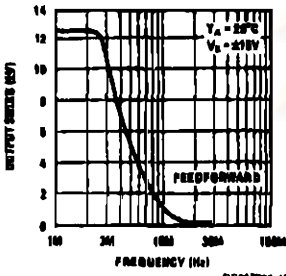**Large Signal Frequency Response**

DS007766-37

Open Loop Frequency Response
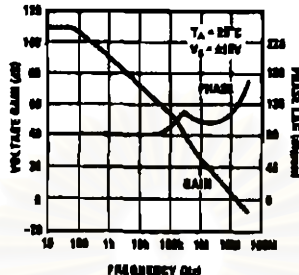
DS007766-38

Voltage Follower Pulse Response

DS007766-39

Large Signal Frequency Response

DS007766-40

Open Loop Frequency Response
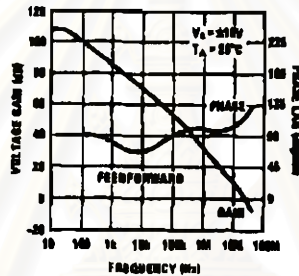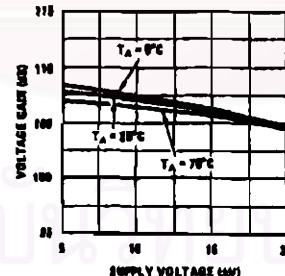

DS007766-41

Inverter Pulse Response
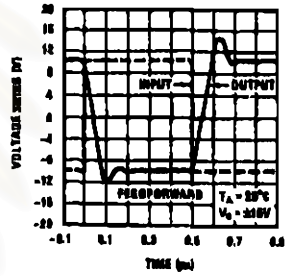
DS007766-42
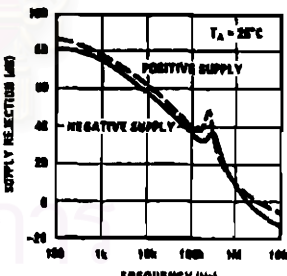
Typical Performance Characteristics LM318

Input Current
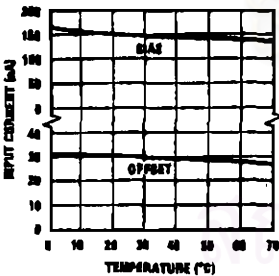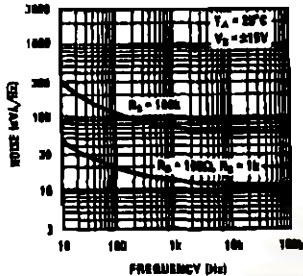

DS007766-43

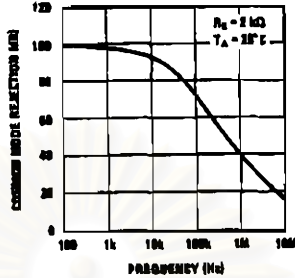**Voltage Gain**

DS007766-44

Power Supply Rejection

DS007766-45

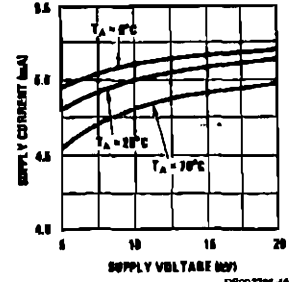# Typical Performance Characteristics LM318 (Continued)

Input Noise Voltage

Common Mode Rejection

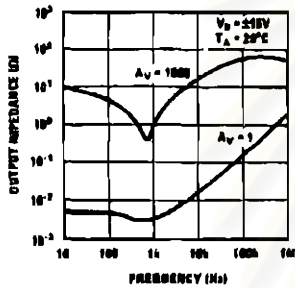**Supply Current**

Closed Loop Output Impedance

Current Limiting

Input Current

Unity Gain Bandwidth

Voltage Follower Slew Rate

Inverter Settling Time

Typical Performance Characteristics LM318 (Continued)

Large Signal Frequency Response

DS007766-55

Open Loop Frequency Response

DS007766-56

Voltage Follower Pulse Response

DS007766-57

Large Signal Frequency Response

DS007766-58

Open Loop Frequency Response

DS007766-59

Inverter Pulse Response

DS007766-60
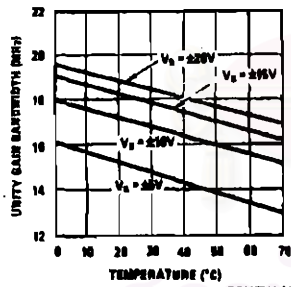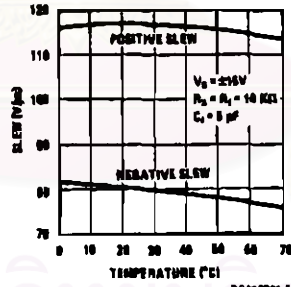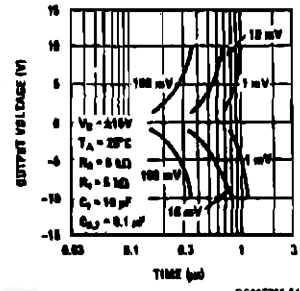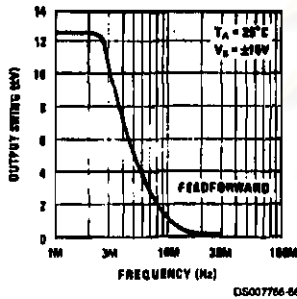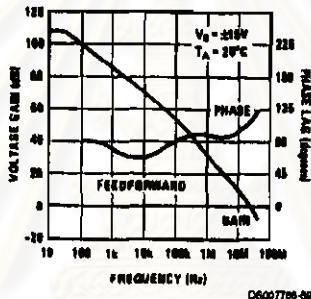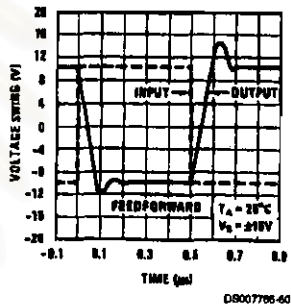
Auxiliary Circuits

Feedforward Compensation for Greater Inverting Slew Rate
(Note 10)

DS007766-8

*Balance circuit necessary for increased slew.

Note 10: Slew rate typically 150V/µs.

Compensation for Minimum Settling Time
(Note 11)

DS007766-9

Note 11: Slew and settling time to 0.1% for a 10V step change is 600 ns.

1MHz, Four Quadrant Analog Multiplier

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

Pinout

**ICL8013
(METAL CAN)
TOP VIEW**
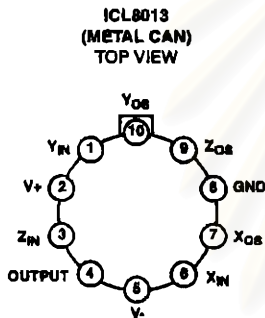
Features

- Accuracy .... ±0.5% ("A" Version)
- Input Voltage Range .... ±10V
- Bandwidth 1MHz
- Uses Standard ±15V Supplies
- Built-In Op Amp Provides Level Shifting, Division and Square Root Functions

Ordering Information

PART NUMBER	MULTIPLI- CATION ERROR (MAX)	TEMP. RANGE (°C)	PKG	PKG. NO.
ICL8013ACTX	±0.5%	0 to 70	10 Pin Metal Can	T10.B
ICL8013BCTX	±1%	0 to 70	10 Pin Metal Can	T10.B
ICL8013CCTX	±2%	0 to 70	10 Pin Metal Can	T10.B

Functional Diagram
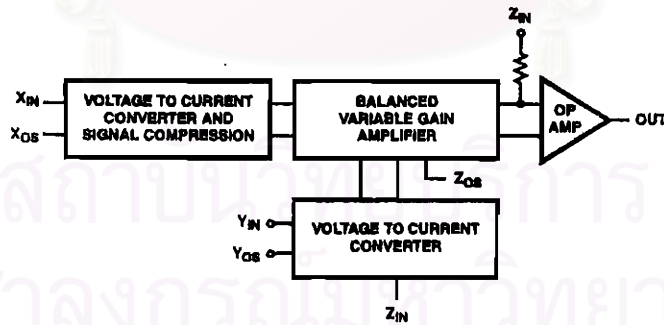
ICL8013

Absolute Maximum Ratings

Supply Voltage.................................... ±18
Input Voltages (X_{IN}, Y_{IN}, Z_{IN}, X_{OS}, Y_{OS}, Z_{OS}) .... V_{SUPPLY}

Operating Conditions

Temperature Range
  ICL8013XC................................... 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	160	75

Maximum Junction Temperature (Metal Can Package).......175°C
Maximum Storage Temperature Range.......... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .... 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C, V_{SUPPLY} = ±15V, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function		-	$\frac{XY}{10}$	-	-	$\frac{XY}{10}$	-	-	$\frac{XY}{10}$	-	
Multiplication Error	-10 < X < 10 -10 < Y < 10	-	-	0.5	-	-	1.0	-	-	2.0	% Full Scale
Divider Function		-	$\frac{10Z}{X}$	-	-	$\frac{10Z}{X}$	-	-	$\frac{10Z}{X}$	-	
Division Error	X = -10	-	0.3	-	-	0.3	-	-	0.3	-	% Full Scale
	X = -1	-	1.5	-	-	1.5	-	-	1.5	-	% Full Scale
Feedthrough	X = 0, Y = ±10V	-	-	50	-	-	100	-	-	200	mV
	Y = 0, X = ±10V	-	-	50	-	-	100	-	-	150	mV
Non-Linearity		-	-	-	-	-	-	-	-	-	
X Input	X = 20V$_{P-P}$ Y = ±10V$_{DC}$		±0.5			±0.5			±0.8		%
Y Input	Y = 20V$_{P-P}$ X = ±10V$_{DC}$	-	±0.2	-	-	±0.2	-	-	±0.3	-	%
Frequency Response Small Signal Bandwidth (-3dB)		-	1.0	-	-	1.0	-	-	1.0	-	MHz
Full Power Bandwidth		-	750	-	-	750	-	-	750	-	kHz
Slew Rate		-	45	-	-	45	-	-	45	-	V/µs
1% Amplitude Error		-	75	-	-	75	-	-	75	-	kHz
1% Vector Error (0.5° Phase Shift)		-	5	-	-	5	-	-	5	-	kHz
Settling Time (to ±2% of Final Value)	V_{IN} = ±10V	-	1	-	-	1	-	-	1	-	µs
Overload Recovery (to ±2% of Final Value)	V_{IN} = ±10V	-	1	-	-	1	-	-	1	-	µs
Output Noise	5Hz to 10kHz	-	0.6	-	-	0.6	-	-	0.6	-	mV$_{RMS}$
	5Hz to 5MHz	-	3	-	-	3	-	-	3	-	mV$_{RMS}$
Input Resistance											
X Input	V_{IN} = 0V		10			10			10		MΩ
Y Input		-	6	-	-	6	-	-	6	-	MΩ
Z Input		-	36	-	-	36	-	-	36	-	kΩ

ICL8013

Electrical Specifications $T_A = 25^{\circ}C$, $V_{SUPPLY} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Bias Current		•	•	•	•	•		•	•		
X or Y Input	$V_{IN} = 0V$	-	2	5			7.5			10	µA
Z Input		-	25	-	-	25	-	-	25	-	µA
Power Supply Variation		•		•	•		•	•	•	•	
Multiplication Error		-	0.2			0.2			0.2		%/%
Output Offset		-	-	50	-	-	75	-	-	100	mV/V
Scale Factor		-	0.1	-	-	0.1	-	-	0.1	-	%/%
Quiescent Current		-	3.5	6.0	-	3.5	6.0	•	3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	$-10V < X_{IN} < 10V$, $-10V < Y_{IN} < 10V$	•	1.5	•	-	2	-	-	3	-	% Full Scale
Average Temp. Coefficients		•		•	Ŀ		•	•		•	
Accuracy			0.06			0.06			0.06		%/°C
Output Offset		-	0.2	-	-	0.2	-	-	0.2	-	mV/°C
Scale Factor		-	0.04	-	-	0.04	-	-	0.04	-	%/°C
Input Bias Current		•	•		•	•		•	•		
X or Y Input	$V_{IN} = 0V$			5			5			10	µA
Z Input		-	-	25	-	-	25	-	-	35	µA
Input Voltage (X, Y, or Z)		-	•	±10	•	•	±10	•	-	±10	V
Output Voltage Swing	$R_L \geq 2k\Omega$ $C_L < 1000pF$	-	±10	-	•	±10	-	•	±10	•	V

Schematic Diagram
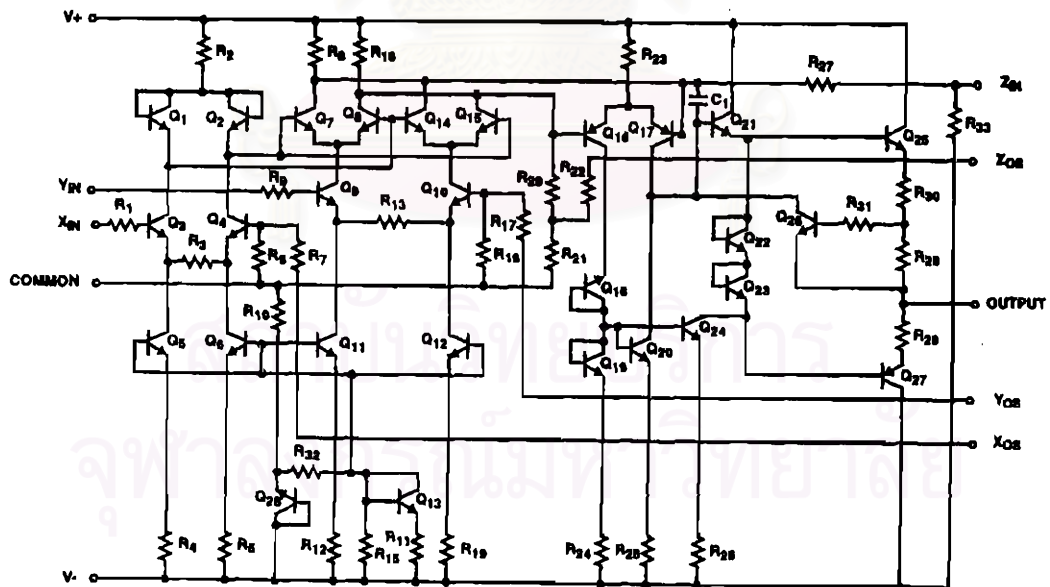
Application Information

Detailed Circuit Description

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.
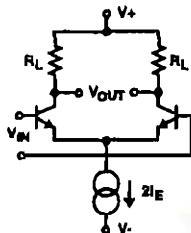

FIGURE 1. DIFFERENTIAL AMPLIFIER

The small signal differential voltage gain of this circuit is given by:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_E}$$

Substituting $r_E = \frac{1}{g_M} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\left(\frac{R_L}{r_E}\right) = V_{IN} \times \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D = \frac{V_Y}{R_Y} = 2I_E \text{ and}$$
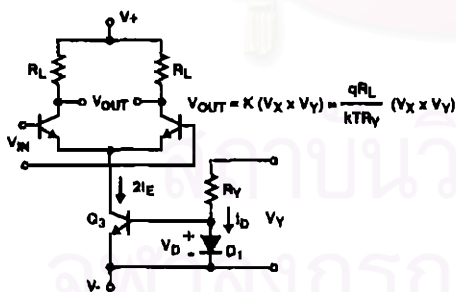
$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \times V_Y)$$

FIGURE 2. TRANSCONDUCTANCE MULTIPLIER

There are several difficulties with this simple modulator:

1. V_Y must be positive and greater than V_D.
2. Some portion of the signal at V_X will appear at the output unless $I_E = 0$.
3. V_X must be a small signal for the differential pair to be linear.
4. The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0V to ±10V with excellent linearity.
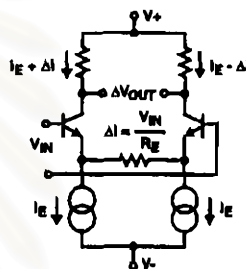

FIGURE 3. VOLTAGE TO CURRENT CONVERTER

The second problem is called feedthrough; i.e., the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, 4B, and 4C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in Figure 4A of exactly equal current sources basing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2} the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage
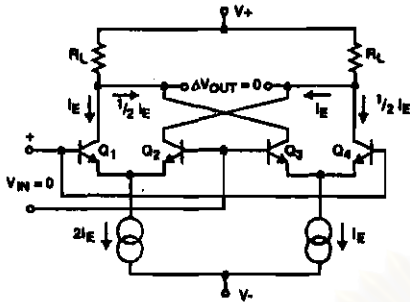
ICL8013

FIGURE 4B. NO INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$

to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).
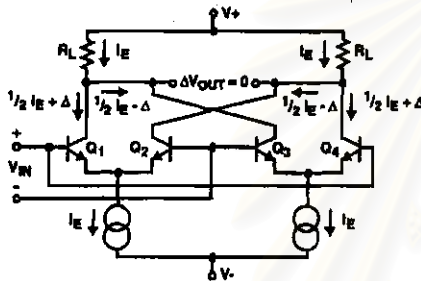

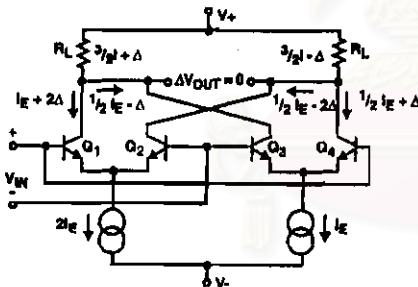**FIGURE 4A. INPUT SIGNAL WITH BALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$**

FIGURE 4C. INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES, DIFFERENTIAL OUTPUT VOLTAGE

This circuit of Figure 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.
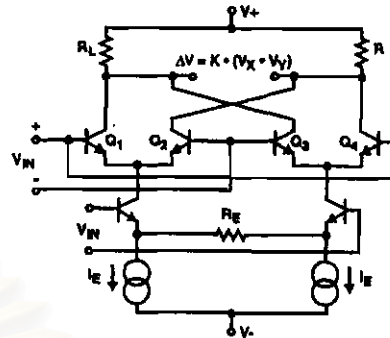

FIGURE 5. TYPICAL FOUR QUADRANT MULTIPLIER-MODULATOR

Figure 2 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 3, we have Figure 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown after the Electrical Specifications Table. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.
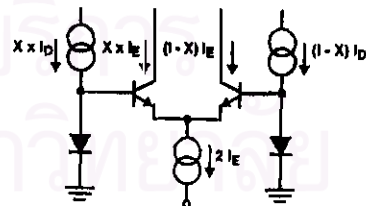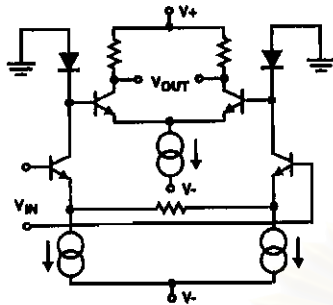

FIGURE 6A. CURRENT GAIN CELL

ICL8013

FIGURE 6B. VOLTAGE GAIN WITH SIGNAL COMPRESSION

FIGURE 7A. MULTIPLIER BLOCK DIAGRAM

FIGURE 7B. MULTIPLIER CIRCUIT CONNECTION

Definition of Terms

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through it nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

Typical Applications

Multiplication

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R_{27} and produces a proportional output voltage.

MULTIPLIER TRIMMING PROCEDURE

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.

2. Apply a $\pm 10V$ low frequency ($\leq 100Hz$) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.

3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.

4. Readjust Z_{OS} as in Step 1, if necessary.

5. With $X_{IN} = 10.0V_{DC}$ and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A+B) by inverting one signal and adjusting Gain control for (Output - Y_{IN}) = Zero.
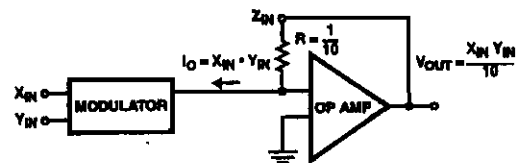
Division

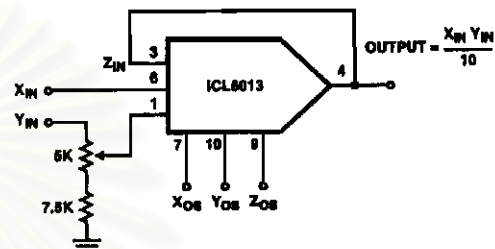If the Z terminal is used as an input, and the output of the op amp connected to the Y input, the device functions as a divider. Since the input to the op amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X_{IN} \cdot Y_{IN} = \frac{Z_{IN}}{R} = 10 Z_{IN}$$

$$\text{Since } Y_{IN} = V_{OUT}, V_{OUT} = \frac{10 Z_{IN}}{X_{IN}}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

DIVIDER TRIMMING PROCEDURE

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for 0V.

2. With $Z_{IN} = 0V$, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from -10V through -1V.

3. With $Z_{IN} = 0V$ and $X_{IN} = -10.0V$ adjust Y_{OS} for zero Output voltage.

4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst case variation of Output, as X_{IN} is varied from -10V to -1V.

5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.

6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (-10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from -10V to -3V.
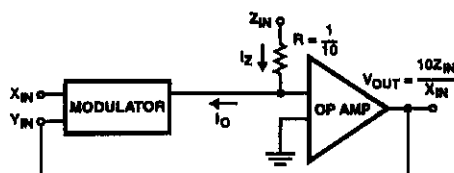
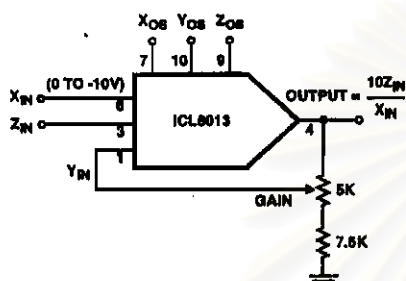# ICL8013

FIGURE 8A. DIVISION BLOCK DIAGRAM

FIGURE 8B. DIVISION CIRCUIT CONNECTION

Squaring

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2 \omega t = \frac{1}{2} (\cos 2\omega t + 1)$.
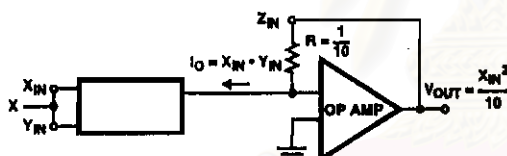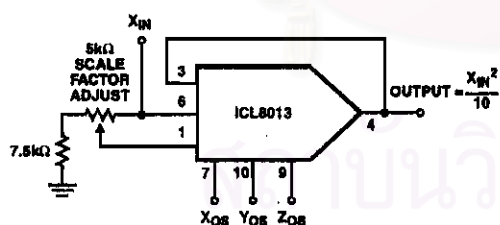

FIGURE 9A. SQUARER BLOCK DIAGRAM

FIGURE 9B. SQUARER CIRCUIT CONNECTION

Square Root

Tying the X and Y inputs together and using overall feedback from the op amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} \times Y_{IN} = (-V_{OUT})^2 = 10Z_{IN}$$

$$V_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the op amp output prevents the latchup that would otherwise occur for negative input voltages.

SQUARE ROOT TRIMMING PROCEDURE

1. Connect the ICL8013 in the Divider configuration.

2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.

3. Convert to the Square Root configuration by connecting X_{IN} to the output and inserting a diode between Pin 4 and the output node.

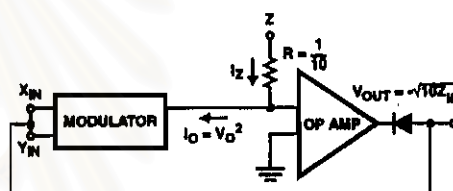4. With $Z_{IN} = 0V$ adjust Z_{OS} for zero output voltage.
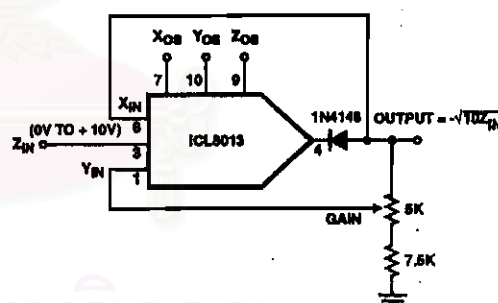

FIGURE 10A. SQUARE ROOT BLOCK DIAGRAM

FIGURE 10B. ACTUAL CIRCUIT CONNECTION

Variable Gain Amplifier

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with

ICL8013

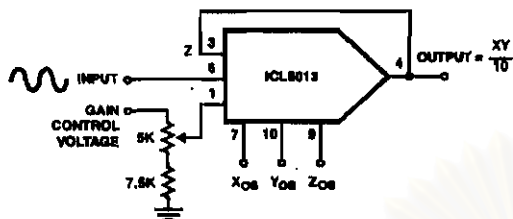the input signal applied at the X input and the control voltage applied at the Y input.
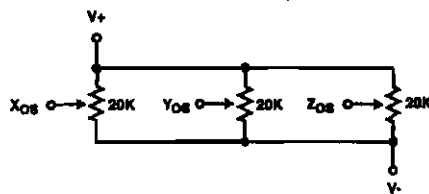

FIGURE 11. VARIABLE GAIN AMPLIFIER

FIGURE 12. POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH
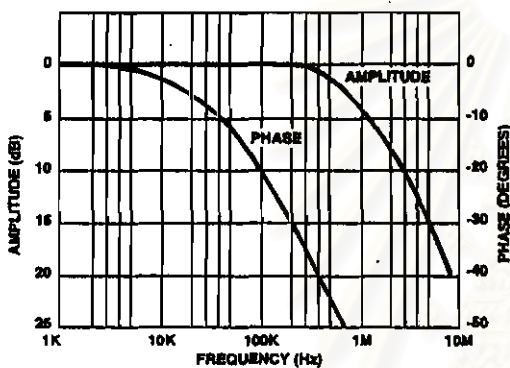
Typical Performance Curves
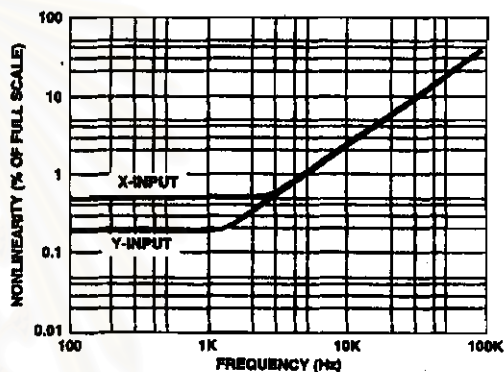

FIGURE 13. FREQUENCY RESPONSE
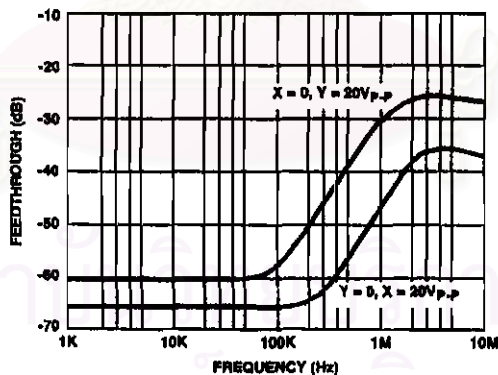

FIGURE 14. NONLINEARITY vs FREQUENCY

FIGURE 15. FEEDTHROUGH vs FREQUENCY

ประวัติผู้เขียน

นายอดิศักดิ์ ปัญญานุช เกิดวันที่ 16 เมษายน พ.ศ. 2515 ปีชวด ที่อำเภอเมือง จังหวัดสมุทรปราการ สำเร็จการศึกษาปริญญาตรีอุตสาหกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์ มหาวิทยาลัยศรีนครินทรวิโรฒ ประสานมิตร ในปีการศึกษา 2537 เข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตรมหาบัณฑิต สาขานิวเคลียร์เทคโนโลยี เมื่อ พ.ศ. 2538